

ABSTRACT OF THE DISCLOSURE

[0052] One embodiment of a distributed memory module cache includes tag memory and associated logic implemented at the memory controller end of a memory channel. The memory controller is coupled to at least one memory module by way of a point-to-point interface. The data cache and associated logic are located in one or more buffer components on each of the memory modules. The memory controller communicates with the memory module via a variety of commands. Included in these commands are an activate command and a cache fetch command. A command is delivered from the memory controller to the memory modules over four transfer periods. The activate command and the cache fetch command have formats that differ only in the information delivered in the fourth transfer period. A read command and a read and preload command similarly differ only in the information delivered over the fourth transfer period. Differentiating different commands during the fourth transfer period allows the maximum amount of time to process tag look-ups.

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